O.P.Code: 16EC431	R16	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech IV Year I Semester Supplementary Examinations June-2024
VLSI DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	List out the steps involved in n-well CMOS process.	CO1	L3	6M
	b	Design the circuit diagram of a simple BiCMOS inverter and explain its operation.	CO1	L4	6M
		OR			
2		Analyze the different types of alternative pull-ups with neat sketches.	CO1	L4	12M

UNIT-II

3	a	Explain the different steps involved VLSI Design flow.	CO2	L2	6M
	b	Develop the schematic and layout for 2-input NAND gate.	CO2	L4	6M
		OR			
4	a	Explain design rules for wires and MOS transistors.	CO2	L2	6M
	b	Draw the stick diagram for Y= (AB+CD)' using NMOS design style.	CO2	L4	6M

UNIT-III

5		Elaborate the following below a) Floorplanning b) Placement c) Routing	CO3	L2	12M
		OR			
6	a	Design the 2 input NAND gate by using pseudo NMOS logic.	CO3	L4	6M
	b	Explain about pass transistors and transmission gate.	CO3	L2	6M

UNIT-IV

7	a	Design and Explain the circuit diagram of four bit Carry ripple adder.	CO4	L4	6M
	b	Explain about 4 transistor Dynamic memory cell.	CO4	L3	6M
		OR			
8		Design a Arithmetic and Logic Unit circuit with four functions by using multiplexer logic.	CO4	L4	12M

UNIT-V

9	a	Discuss in detail about standard cell design with suitable diagrams.	CO5	L2	6M
	b	What is testing? And explain any three test principles.	CO5	L2	6M
		OR			
10		Design the logic diagram of PLA for the following. Y1=A'B'C'+ABC+A'B+ABC' Y2=ABC+A'B'C+AC Y3=A'BC'+AB'C+B'C'	CO5	L5	12M

***** END *****